In the Drawings

Please replace drawing sheet 2/7 with the attached replacement sheet 2/7. In this replacement sheet, the element "H50" replaces element "L50" extending vertically above top surface 21 in FIG. 1B. Applicants' specification at paragraph [0021] supports the correction of this typographical error.

Remarks

Claims 1-16 and 20-21 are in the application. Claims 17-19 have been cancelled.

By this amendment, applicants have amended claims 1-5, 8, and 13-15 to more particularly point out and distinctly claim the subject matter of their invention. The specification including paragraphs [0016] and [0019] and FIGS. 1, 1A, and 1B support the changes to claim 1. The specification including paragraph [0017] and FIG. 1A supports the changes to claims 2 and 14. The specification including paragraph [0022] and FIG. 2 supports the changes to claim 3. The specification including paragraph [0020] and FIG. 1B supports the changes to claim 4. The specification including FIG. 1 supports the changes to claims 5 and 8. the specification including paragraphs [0016] and [0019] and FIGS. 1, 1A, and 1B support the changes to claim 13. Claim 7 has been amended to have proper antecedent basis in view of the changes to claim 1.

Additionally, new claims 20 and 21 have been added. The specification including paragraphs [0019]-[0022] and FIG. 2 support the addition of the new claims.

Moreover, applicants have amended paragraphs [0011] and [0019] to correct minor typographical errors. Further, applicants are submitting herewith a Replacement Sheet 2/7 where element "H50" is added to FIG. 1B to replace element "L50". Applicants' specification including paragraph [0021] support the change to drawing sheet 2/7.

Claims 1, 2, 4-7 and 9-14 were rejected under 35 U.S.C. §102(b) as being anticipated by Yakida, Japanese Patent #10-289921 ("Yakida"). This rejection is respectfully traversed in view of the amendments made herein and the remarks presented hereinafter.

Claim 1 calls for a semiconductor device, comprising a semiconductor die having first and second bonding pads formed on a major surface and further having first and second edges. A first inductor including a first bonding wire is attached at one end to the first bonding pad and at a second end to the second bonding pad. The first inductor extends laterally a distance greater than a height of the bonding wire to define an insulating core. Additionally, the first inductor projects laterally over the first edge of the semiconductor die at least at two locations.

Applicants respectfully submit that Yakida fails to anticipate claim 1 because Yakida does not teach a first inductor that projects laterally over the first edge of the semiconductor die at least at two locations. As is evident in all of Yakida's figures, his inductors lie solely above the major surface of his semiconductor die and do not project laterally over any edges.

Claims 2, 4-7 and 9-12 depend from claim 1 and are believed allowable for at least the same reasons as claim 1.

Claim 13 calls for a semiconductor device, comprising a semiconductor die having a plurality of bonding pads on a major surface and an edge. A first inductor comprising a first bonding wire is formed in a coil around a dielectric core, and has a first end coupled to a first bonding pad on the major surface and a second end coupled to a second bonding pad on the major surface. Further, the first inductor projects over the edge of the semiconductor die a lateral distance greater than its height, and the first inductor projects laterally over the edge at least at two locations.

Applicants respectfully submit that Yakida fails to anticipate claim 13 because Yakida does not teach a first inductor that projects over an edge of the semiconductor die a lateral distance greater than its height. As is evident in all

of Yakida's figures, his inductors lie solely above the major surface of his semiconductor die and do not project over any edge.

Claim 14 depends from claim 13 and is believed allowable for at least the same reasons as claim 13.

Claims 1, 4-8, 12, 13 and 16 were rejected under 35 U.S.C. §102(b) as being anticipated by Japanese Patent No. 06140451 assigned to Hitachi LTD (hereafter "Hitachi"). This rejection is respectfully traversed in view of the amendments made herein and the remarks presented hereinafter.

Claim 1 calls for a semiconductor device, comprising a semiconductor die having first and second bonding pads formed on a major surface and further having first and second edges. A first inductor including a first bonding wire is attached at one end to the first bonding pad and at a second end to the second bond pad. The first inductor extends laterally a distance greater than a height of the bonding wire to define an insulating core. Additionally, the first inductor projects laterally over the first edge of the semiconductor die at least at two locations.

Applicants respectfully submit that the Hitachi reference fails to anticipate claim 1 because it does not teach a first bonding wire attached at one end to a first bonding pad on a semiconductor die and at a second end to a second bonding pad on the semiconductor die. In the Hitachi reference, only one end is attached to a bonding pad on the semiconductor die. Additionally, the Hitachi reference does not teach a first inductor that projects laterally over the first edge of the semiconductor die at least at two locations. In particular, the Hitachi reference teaches an inductor that projects laterally over the edge at one location only.

Claims 4-8 and 12 depend from claim 1 and are believed allowable for at least the same reasons as claim 1.

Claim 13 calls for a semiconductor device, comprising a semiconductor die having a plurality of bonding pads on a major surface and an edge. A first inductor comprising a first bonding wire is formed in a coil around a dielectric core, and has a first end coupled to a first bonding pad on the major surface and a second end coupled to a second bonding pad on the major surface. Further, the first inductor projects over the edge of the semiconductor die a lateral distance greater than its height, and the first inductor projects laterally over the edge at least at two locations.

Applicants respectfully submit that the Hitachi reference fails to anticipate claim 13 because it does not teach a first inductor having a first end coupled to a bonding pad on the major surface and a second end couple to a second bonding pad on the major surface. In the Hitachi reference, the inductor is coupled at one end to a bonding pad on the semiconductor die and at the second end to a package lead.

Claim 16 depends from claim 13 and is believed allowable for at least the same reasons as claim 13.

Claims 1, 2, 4, and 7 were rejected under 35 U.S.C. §102(b) as being anticipated by Van Schulenbergh et al., European Patent 1, 202 296 A1, (hereinafter "'296"). This rejection is respectfully traversed in view of the amendments made herein and the remarks presented hereinafter.

Claim 1 calls for a semiconductor device, comprising a semiconductor die having first and second bonding pads formed on a major surface and further having first and second edges. A first inductor including a first bonding wire is attached at one end to the first bonding pad and at a second end to the second

bond pad. The first inductor extends laterally a distance greater than a height of the bonding wire to define an insulating core. Additionally, the first inductor projects laterally over the first edge of the semiconductor die at least at two locations.

Applicants respectfully submit that the '296 reference fails to anticipate claim 1 because it does not teach a first inductor that projects laterally over the first edge of the semiconductor die at least at two locations. In particular, the '296 reference teaches inductors that lie solely above the major surface of the semiconductor die. Morever, the '296 reference does not teach a first inductor that extends laterally a distance greater than the height of the bonding wire to define an insulating core. Specifically, from the '296 drawings, the lateral distance of each '296 inductor appears to be equal to or less than the height thereof.

Claims 2, 4, and 7 depend from the claim 1 and are believed allowable for at least the same reasons as claim 1.

Claims 1, 2, and 6-14 were rejected under 35 U.S.C. §102(b) as being anticipated by Lee et al., USP 6,775,901, (hereinafter "Lee"). This rejection is respectfully traversed in view of the amendments made herein and the remarks presented hereinafter.

Claim 1 calls for a semiconductor device, comprising a semiconductor die having first and second bonding pads formed on a major surface and further having first and second edges. A first inductor including a first bonding wire is attached at one end to the first bonding pad and at a second end to the second bond pad. The first inductor extends laterally a distance greater than a height of the bonding wire to define an insulating core. Additionally, the first inductor projects laterally over the first edge of the semiconductor die at least at two locations.

Applicants respectfully submit that Lee fails to anticipate claim 1 because it does not teach a first inductor that projects laterally over the first edge of the semiconductor die at least at two locations. In particular, the Lee reference teaches inductors that lie solely above the major surface of the semiconductor die and do not project laterally over any edge.

Claims 2 and 6-12 depend from claim 1 and are believed allowable for at least the same reasons as claim 1.

Claim 13 calls for a semiconductor device, comprising a semiconductor die having a plurality of bonding pads on a major surface and an edge. A first inductor comprising a first bonding wire is formed in a coil around a dielectric core, and has a first end coupled to a first bonding pad on the major surface and a second end coupled to a second bonding pad on the major surface. Further, the first inductor projects over the edge of the semiconductor die a lateral distance greater than its height, and the first inductor projects laterally over the edge at least at two locations.

Applicants respectfully submit that Lee fails to anticipate claim 13 because Lee does not teach a first inductor that projects over an edge of the semiconductor die a lateral distance greater than its height. As is evident in all of Lee's figures, his inductors lie solely above the major surface of his semiconductor die and do not project over any edge.

Claim 14 depends from claim 13 and is believed allowable for at least the same reasons as claim 13.

Claims 3 and 15 were rejected under 35 U.S.C. §103(a) as being obvious over Yakida in view of the Hitachi reference. This rejection is respectfully traversed in view of the amendments made herein and the remarks presented hereinafter.

Claim 3 depends from claim 1, and applicants will first respond to the §103 rejection in view of claim 1. Claim 1 calls for a semiconductor device, comprising a semiconductor die having first and second bonding pads formed on a major surface and further having first and second edges. A first inductor including a first bonding wire is attached at one end to the first bonding pad and at a second end to the second bond pad. The first inductor extends laterally a distance greater than a height of the bonding wire to define an insulating core. Additionally, the first inductor projects laterally over the first edge of the semiconductor die at least at two locations.

Applicants respectfully submit that the proposed combination fails to satisfy all limitations of claim 1. First, the Yakida reference fails to show or suggest a first inductor that extends laterally over a first edge of a semiconductor die. In Yakida, all inductors lie directly above the major surface of his semiconductor die. Moreover, the only bonding wires extending over the edge of Yakida's semiconductor die are conventional straight wire bonds, and each does so at one location only.

The Hitachi reference teaches a wire bond formed as an coiled inductor connecting a semiconductor die to a conductive lead only, and as a result, the only motivation Yakida and the Hitachi reference in combination suggest is to replace Yakida's wire bonds 4 with the Hitachi 12 coiled inductor wire bond, which would still only have one location that passes over the edge of the Yakida semiconductor die. However, this falls short of the limitation that requires a first inductor that projects laterally over an edge of the semiconductor die at least at two locations.

Applicants respectfully submit that this is not a minor difference. As stated in their specification including paragraphs [0018]-[0021], their configuration provides a low package profile while reducing parasitic effects from conductive regions on the semiconductor die. Thus, for at least these

reason, applicants respectfully submit that claim 1 is allowable over Yakida in view of the Hitachi reference.

Claim 3 depends from claim 1 and further calls for first and second leads in spaced relationship with the semiconductor die, and, a second inductor including a second bonding wire attached at one end to the first lead and attached at a second end to the second lead. Claim 3 is believed allowable for the same reasons as claim 1. Additionally, applicants respectfully submit that the combination of references fails to show or suggest a second inductor including a second bonding wire attached at one end to the first lead and attached at a second end to the second lead.

Claim 15 depends from claim 13. Claim 13 calls for a semiconductor device, comprising a semiconductor die having a plurality of bonding pads on a major surface and an edge. A first inductor comprising a first bonding wire is formed in a coil around a dielectric core, and has a first end coupled to a first bonding pad on the major surface and a second end coupled to a second bonding pad on the major surface. Further, the first inductor projects over the edge of the semiconductor die a lateral distance greater than its height, and the first inductor projects laterally over the edge at least at two locations.

Applicants respectfully submit that the proposed combination fails to satisfy all limitations of claim 13. First, the Yakida reference fails to show or suggest a first inductor that extends laterally over an edge of a semiconductor die. In Yakida, all inductors lie directly above the major surface of his semiconductor die. Moreover, the only bonding wires extending over the edge of Yakida's semiconductor die are conventional straight wire bonds, and each does so at one location only.

The Hitachi reference teaches a wire bond formed as an coiled inductor connecting a semiconductor die to a conductive lead only, and as a result, the only motivation Yakida and the

Hitachi reference in combination suggest is to replace Yakida's wire bonds 4 with the Hitachi 12 coiled inductor wire bond, which would still only have one location that passes over the edge of the Yakida semiconductor die. However, this falls short of the limitation that requires a first inductor that projects laterally over an edge of the semiconductor die at least at two locations.

Applicants respectfully submit that this is not a minor difference. As stated in their specification including paragraphs [0018]-[0021], their configuration provides a low package profile while reducing parasitic effects from conductive regions on the semiconductor die. Thus, for at least these reason, applicants respectfully submit that claim 13 is allowable over Yakida in view of the Hitachi reference.

Claim 15 depends from claim 13 and further calls for the dielectric core is substantially centered along an axis running parallel to the edge. Claim 15 is believed allowable for at least the same reasons as claim 13. Additionally, applicants respectfully submit the combination of references still falls short of showing or suggesting a dielectric core substantially centered along an axis running parallel to the edge the inductor lateral extends over.

New claim 20 depends from claim 3 and applicants further submit that is allowable for at least the same reasons as claims 1 and 3. Additionally, claim 21 depends from claim 13 and applicants respectfully believe this claim is allowable for at least the same reasons as claim 13.

Applicants respectfully believe that in view of the cancellation of claims 17-19, no fee is due for new claims 20 and 21. However, applicants hereby authorize the Commissioner to charge deposit account 501086 for any fees due, or to credit the same account for any refunds or credits due.

In view of all of the above, it is believed that the claims are allowable, and the case is in condition for allowance, which action is earnestly solicited.

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